REMARKS

Claims 5-7, 16 and 17 were pending in the application. By this amendment, claims 5-7, 16 and 17 are being cancelled without prejudice, and are being replaced by new claims 18-21, to advance the prosecution of the application. No new matter is involved.

In the final Office Action of March 15, 2002, claims 5-7, 16 and 17 are rejected on prior art. More specifically, claims 16, 17, 5 and 6 are rejected under 35 U.S.C. § 103(a) as unpatentable over Sato in view of Mori. Claim 7 is rejected under 35 U.S.C. § 103(a) as unpatentable over Sato in view of Mori and taken with Santin. These rejections are respectfully traversed. However, the rejected claims are being replaced by new claims 18-21 which set forth the features according to the present invention in a manner which clearly distinguishes patentably over the prior art.

Addressing first the Sato reference, the present invention relates to a semiconductor memory device having an STI structure. Sato, on the other hand, relates to a semiconductor memory device having a LOCOS structure. The basic structure of the semiconductor device according to the present invention is significantly different from that of Sato.

More particularly, in the case of the present invention, portions near the surface of the semiconductor substrate are isolated by strip-shaped STI layers, and memory regions are formed in the areas between the adjacent STI layers. Memory transistors are formed in these memory regions. In Sato, the device isolation is performed by

LOCOS. There is no STI layer. Therefore, the manner of isolating devices in the case of the present invention is significantly different from that in Sato.

Moreover, the manner of connecting the source/drain diffusion layer and the metal wiring in the case of the present invention is significantly different from that in Sato. The oxide layer (LOCOS) used for device isolation in Sato is removed to connect the sources of memory cells. In contrast, and in the case of the present invention, the SiN stopper layer is used to prevent etching of the oxide layer (STI) used for device isolation at both the drain side and the source side. The SiN stopper layer is neither directly nor indirectly disclosed in Sato.

Therefore, structures in accordance with the present invention are remarkably different from those disclosed in Sato. The present invention is neither disclosed nor suggested by Sato.

Addressing the Mori reference, the sidewall portion of Mori is considerably different technically from that of the present invention. Those skilled in the art will appreciate such differences from a technical analysis standpoint, and will appreciate that the present invention cannot be arrived at based on the teaching of Mori.

More particularly, in Mori, an O-N-O three-layer structure, which includes the oxide layer (O) 37, the nitride layer (N) 36, and the oxide layer (O) 29, is provided to the inside of the third SiN layer 30. In other words, the portion between the SiN layer 30 and the gate polycrystalline silicon layer 23, 23a, result in the gate polycrystalline silicon layer 23, 23a, the SiO_2 layer 29, the SiN layer 36, and the SiO_2 layer 37, and the SiN layer 30, being arranged in this order. This is because when a

positive voltage is applied to the plug 32, holes are trapped in the nitride layer 30, entry of the holes into the SiN layer 36 is prevented by the oxide layer 36, and accordingly, the electrons in the floating gate are prevent from emitting, thereby enabling the storage of data.

In contrast, and in the case of the present invention, the oxide layer 32 serves as an etching stopper at the time of the etching of the SiN layer 10, as shown, for example, in Figs. 6(a), 6(b), 7(a), and 7(b).

Therefore, the technical significance of the oxide layer in accordance with the present invention is significantly different from that in Mori. Those skilled in the art could not achieve the present invention based on the teaching of Mori.

Further in accordance with the present invention, silicidation is performed. Before performing the silicidation, it is necessary to expose the silicon at the surface of the diffusion layer so as to cause the silicon to react with the metal layer. The process flow comprises the removal of the layer at the surface of the diffusion layer, the deposition of the metal layer, the silicidation, the deposition of the etching stopper layer, and the formation of the contact. In Mori, the SiO_2/SiN/SiO_2 layers which proposed are formed before the silicidation process. Therefore, these layers should be removed before the silicidation process, and cannot serve as an etching stopper.

New claims 18-21 are submitted to clearly distinguish patentably over the attempted combination of prior art references.

Claim 18 defines a nonvolatile semiconductor memory device which includes strip-shaped isolation layers embedded in a surface of a semiconductor substrate, with

a strip-shaped memory region formed between two adjacent isolation layers, and with the adjacent memory regions being isolated by an isolation layer. The memory transistors formed in each of the memory regions are then defined in detail, in terms of a floating gate, a control gate and two source/drain diffusion layers. The memory device is further defined in terms of sidewalls which are formed by an outside layer serving as a stopper at the time of etching. Layers formed of a second silicon nitride layer are removed by etching so as not to exist on the source/drain diffusion layers, so that the source/drain diffusion layers are exposed. Therefore, claim 1 is submitted to clearly distinguish patentably over the attempted combination of prior art references. The prior art references are discussed in detail above in terms of the manner in which they are different from and teach away from the present invention.

Claims 19-21 depend, directly or indirectly, from claim 18, and further define claim 18 in terms of additional details. Claim 19 further defines claim 18 in terms of silicide layers formed on the surfaces of the control gate and the source/drain diffusion layers in each of the memory transistors. Claim 20 further defines claim 19 in terms of one of the source/drain diffusion layers being connected to a bit line via the silicide layer and the other being connected to a common source line via the silicide layer, in each of the memory transistors. Claim 21 further defines claim 18 in terms of at least one of a low-voltage MOS transistor and a high-voltage MOS transistor being formed as a periphery circuit. Therefore, claims 19-21 are submitted to clearly distinguish patentably over the prior art.

In conclusion, new claims 18-21 are submitted to clearly distinguish patentably over the prior art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

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